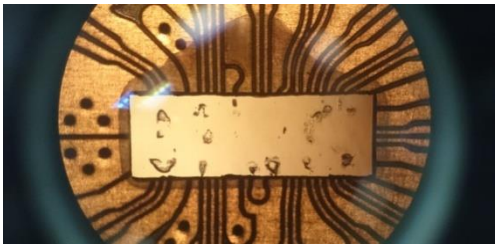
BiFAST
By far the fastest

Preliminary data

40 Gb/s up to 100 Gb/s duobinary 4:1 SERDES chipset

BFDC-100Tx-ES1 & BFDC-100TRx-ES1



- Transmitter (BFDC-100Tx-ES1):
  - 4-way serializer (OIF CEI-25G compatible)
  - 6-tap FFE (stand-alone mode supported)
  - Powerful output buffer ($1V_{pp}$)
  - Control interface: SPI
- Transceiver (BFDC-100TRx-ES1):
  - 4-way serializer and de-serializer (OIF CEI-25G compatible)
  - 6-tap FFE (stand-alone mode supported)
  - Powerful output buffer ($1V_{pp}$)
  - Low-noise duobinary receiver including clock recovery
  - Tunable detection threshold
  - Control interface: SPI

Overview

The BFDC-100Tx-ES1 & BFDC-100TRx-ES1 constitute a chipset implementing 40 Gb/s up to 100 Gb/s duobinary transmission allowing serial communication at data rates of 100 Gb/s across channels with a loss of 40 dB at 50GHz (or 50 Gb/s with a loss of 40 dB at 25 GHz). Both chips come in a small die size (less than $15mm^2$) allowing integration of several dies into a single package alongside an FPGA or core chip. Packaged chips (less than 7x7mm) fit within QSFP28 form factor, cable assemblies and optics modules. The incorporated four-to-one OIF CEI-25G compatible serializer and one-to-four OIF CEI-25G compatible de-serializer provide in- and outputs running at 10 Gb/s up to 25 Gb/s. The 6-tap FFE can be used stand-alone for testing purposes or in case no serialization is needed. The transceiver chipset achieves this performance with a power consumption below 1W including CDR and serialization/de-serialization functionality.

More Information

The BiFAST duobinary 4:1 SERDES chipset is available for private demonstration upon request

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All specifications are subject to change without notice