56+ Gb/s Serial Transmission using Duobinary Signaling
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Introduction
Motivation

- Standard groups looking into serial data rates of 50 Gb/s and above
  - IEEE 802.3bs 400 GbE
    - NRZ and PAM4
  - OIF CEI-56G-VSR/SR (< 100 mm)
    - NRZ and PAM4
  - OIF CEI-56G-MR (500 mm)
    - PAM4

- Duobinary signaling presented as alternative for 56+ Gb/s serial data rates
Overview

- Duobinary signaling
- Duobinary demonstrator
- Design of duobinary chipset
- Measurements
- Conclusions
Duobinary Signaling
Duobinary Signaling

- **NRZ signaling**
  - Requires extensive pre-emphasis or equalization
  - Difficult to scale to data rates beyond 40 Gb/s

- **PAM4 signaling**
  - Reduces spectral requirements compared to NRZ
  - Requires less pre-emphasis and equalization than NRZ
  - More complex – multi-level transmitter and receiver
  - Reduced level spacing – less tolerance to noise

- **Duobinary signaling**
  - 3-level modulation scheme
  - Leverages passive channel frequency response for signal shaping
  - Reduces spectral requirements compared to NRZ
  - Requires less pre-emphasis and equalization than NRZ
Duobinary Signaling

- Duobinary transmission system:
  - Data source (binary data transmitter)
  - Duobinary precoder
  - Feed-forward equalizer (FIR filter)
  - Passive channel (backplane)
  - Duobinary to binary converter (rectifier)
  - Binary data receiver
- Equalization effort reduced
  - Main shaping takes place in the channel
  - Duobinary spectrum has null at ½ data rate
  - FIR filter limited to 5-taps

Emphasize high-frequency components
Flatten group delay response
Duobinary Signaling

- Duobinary – correlative coding
  - Each symbol conveys information corresponding to the previous and current bit – partial response
  - Combination results in 3 level waveform
  - Forbidden transitions form rudimentary error detection – not considered here
  - Requires simple precoding at transmitter
- Duobinary PSD
  - Spectrum compressed compared to NRZ
  - Same spectrum as PAM4
  - Relaxes channel design criteria and bandwidth requirements of transceiver IC's

10-TH3 — 56+ Gb/s Serial Transmission using Duobinary Signaling
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Duobinary Demonstrator – Backplane Channel

TX board

FFE

56 Gb/s

28 GHz clock

CHANNEL

RX board

RX

14 Gb/s

Figure 18: ExaMAX® backplane demonstrator.

Figure 19: Losses 13.7 in backplane channel only (red) and total losses of backplane channel + test setup (blue).
Duobinary Demonstrator – Backplane Channel

- ExaMAX® connector system
- 24 lay – 160 mil backpanel
- 18 lay – 94 mil daughter cards
- Megtron 6 board material

- Daughter card trace length = 6”
- Backpanel trace length = 1.7” to 26.75”
- Total length = 13.7” to 38.75”
- 1.3 dB loss per inch at 28 GHz

**Figure 18:** ExaMAX® backplane demonstrator.

**Figure 19:** Losses 13.7 in backplane channel only (red) and total losses of backplane channel + test setup (blue).
Duobinary Demonstrator – Loss

56 Gb/s PPG

56 Gb/s

FFE

28 GHz clock

1.05 dB at 28 GHz

56 Gb/s

5.6 dB at 28 GHz

CHANNEL

RX board

RX

1.05 dB at 28 GHz

3.8 dB at 28 GHz

14 Gb/s

Scope/BERT

TX board

TX

28 GHz clock

1.05 dB at 28 GHz

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Duobinary Demonstrator – Total Channel Loss

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>LOSS at 28 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX board</td>
<td>5.60 dB</td>
</tr>
<tr>
<td>Coax TX board to channel</td>
<td>1.05 dB</td>
</tr>
<tr>
<td>Channel loss</td>
<td>IL [dB]</td>
</tr>
<tr>
<td>Coax channel to RX board</td>
<td>1.05 dB</td>
</tr>
<tr>
<td>RX board</td>
<td>3.80 dB</td>
</tr>
<tr>
<td>Total loss</td>
<td>IL + 11.5 dB</td>
</tr>
</tbody>
</table>

![Graph showing losses vs frequency]
Chip Design – Overview

- Transceiver chain
- Transmitter overview
- Receiver overview
- FFE parameter optimization
Transceiver Chain

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Transmitter Building Blocks

TX output
\[ IN^*(A_1 + A_2 + A_3 + A_4 + A_5) \]

FFE output buffer

750 um Transmission line

From MUX

FFE input buffer

000011010000

10-TH3 — 56+ Gb/s Serial Transmission using Duobinary Signaling
Transmitter Building Blocks

TX output
\[ \text{IN}^* (A_1 + A_2 + A_3 + A_4 + A_5 + D^2 + A_4 + D^3 + A_5 + D^4) \]

FFE output buffer

From MUX

FFE input buffer

750 um Transmission line

000011010000
Transmitter Building Blocks

TX output
$IN^{+}(A_1+2A_2D+A_3D^2+A_4D^3+A_5D^4)$

FFE output buffer

750 um Transmission line

FFE input buffer

From MUX

000011010000
Transmitter Building Blocks

TX output
$IN^*(A_1+A_2D+A_3D^2+A_4D^3+A_5D^4)$

750 um Transmission line

FFE output buffer

From MUX

FFE input buffer

000011010000

10-TH3 — 56+ Gb/s Serial Transmission using Duobinary Signaling
Transmitter Building Blocks

TX output

\[ \text{IN}(A_1 + A_2 \cdot D + A_3 \cdot D^2 + A_4 \cdot D^3 + A_5 \cdot D^4) \]

FFE output buffer

750 um Transmission line

FFE input buffer

From MUX

000011010000

10-TH3 — 56+ Gb/s Serial Transmission using Duobinary Signaling
Transmitter Building Blocks

TX output
IN*(A1+A2*D+A3*D^2+A4*D^3+A5*D^4)

FFE output buffer

750 um Transmission line

FFE input buffer

From MUX

000011010000
Transmitter Building Blocks

TX output
$IN^+(A_1+2A_2D+A_3D^2+A_4D^3+A_5D^4)$

750 um Transmission line

FFE output buffer

From MUX

FFE input buffer

000011010000

10-TH3 — 56+ Gb/s Serial Transmission using Duobinary Signaling
Receiver Overview

10-TH3 — 56+ Gb/s Serial Transmission using Duobinary Signaling
FFE Parameter Estimation

Channel delays, attenuates and reduces the bandwidth of the impulse response

FFE impulse response calculated from frequency response

FFE impulse response after channel propagation
Generating Least-square-error Fit

- Making a linear combination to obtain the best match
1-tap FFE Parameters

56 Gb/s NRZ

56 Gb/s Duobinary

56 Gb/s PAM4

Impulse response

desired - obtained

Desired eye pattern

normalized

 Obtained eye pattern

normalized at output of FFE
2-tap FFE Parameters

56 Gb/s NRZ
56 Gb/s Duobinary
56 Gb/s PAM4

Impulse response
desired - obtained

Desired eye pattern
normalized

Obtained eye pattern
normalized at output of FFE
3-tap FFE Parameters

56 Gb/s NRZ

56 Gb/s Duobinary

56 Gb/s PAM4

Impulse response

desired - obtained

Desired eye pattern

normalized

Obtained eye pattern

normalized at output of FFE
4-tap FFE Parameters

56 Gb/s NRZ

Impulse response
desired - obtained

Desired eye pattern
normalized

Obtained eye pattern
normalized at output of FFE

56 Gb/s Duobinary

56 Gb/s PAM4

56+ Gb/s Serial Transmission using Duobinary Signaling
5-tap FFE Parameters

56 Gb/s NRZ

56 Gb/s Duobinary

56 Gb/s PAM4

Impulse response
desired - obtained

Desired eye pattern
normalized

Obtained eye pattern
normalized at output of FFE
Chip Design – Conclusions

- Design of a 5-tap FFE capable of equalizing a backplane channel into a 56 Gb/s duobinary channel
- Design of a sensitive 56 Gb/s duobinary receiver with built-in DEMUX
- Optimized FFE parameters estimation methodology based on fast frequency-domain measurements and Matlab optimization techniques
Measurements – Overview

- Test setup
- 40 Gb/s BER vs. insertion loss
- 56 Gb/s BER measurements
Test Setup

TX board

56 Gb/s PPG

28 GHz clock

CHANNEL

RX board

Scope/BERT

56 Gb/s

14 Gb/s

56 Gb/s

10-TH3 — 56+ Gb/s Serial Transmission using Duobinary Signaling
BER Measurement Results – 40 Gb/s

- 40 Gb/s transmission across channels ranging from 13.7” to 26.25”

40 Gb/s – 13.7”

28.0 dB at 20 GHz
BER < 1E-12

40 Gb/s – 26.25”

41.3 dB at 20 GHz
BER ≈ 1E-9
Measurements started at 40 Gb/s on the shortest link (13.7 in, 35 cm). The loss at the Nyquist frequency is 28.8 dB, resulting in a vertical and horizontal eye-opening of 18.2 mV and 15 ps (0.6 UI), compared to the maximum output eye-pattern at the transmitter having an eye-opening of 93.4 mV and 19.1 ps (0.76 UI) at 40 Gb/s. Both eye-patterns are shown in figure 20.

This results in error-free (BER < 1E-12) transmission when connected to the duobinary decoder.

- Error-free (BER < 1E-12) up to about 37 dB total link loss (20” channel + test setup) at Nyquist (20 GHz)
- BER ≈ 1E-9 up to about 42 dB total link loss (26.25” channel + test setup) at Nyquist (20 GHz)
BER Measurement Results – 56 Gb/s

- Error-free (BER < 1E-12) operation at 56 Gb/s across 13.7” channel with a total link loss of about 41 dB at 28 GHz

![](image)

56 Gb/s – 13.7”

41.0 dB at 28 GHz
BER < 1E-12
Conclusions
Conclusions

- Selection of duobinary signaling as a modulation format for high-speed serial transmission
- Duobinary demonstrator
- Design of duobinary transceiver chipset
- Measurement results demonstrate 56 Gb/s serial transmission over a state-of-the-art backplane channel is possible using duobinary signaling
  - Limited equalization: 5-taps FFE, no CTLE or DFE
Visit us at booth 817 for a live demo